

## Features

- 184pin, unbuffered dual in-line memory module (UDIMM)
- Fast data transfer rates: PC-2100, PC-2700, PC3-3200
- Single or Dual rank
- 256MB(32Megx64), 512MB (64Meg x 64), 1GB(128 Meg x 64)
- JEDEC standard 2.5V I/O (SSTL\_2 compatible)
- $V_{DD} = V_{DDQ} = 2.5V \pm 0.1V$
- $V_{DDSPD} = 2.3V$  to 3.6V
- Internal, pipelined double data rate (DDR)  $2n$ -prefetch architecture
- Bidirectional data strobe (DQS) transmitted/received with data—that is, source-synchronous data capture
- Differential clock inputs (CK and CK#)
- Multiple internal device banks for concurrent operation
- Single or Dual rank
- Selectable burst lengths (BL) 2, 4, or 8
- Auto precharge option
- Auto refresh and self refresh modes: 7.8125 $\mu$ s maximum average periodic refresh interval
- Serial presence-detect (SPD) with EEPROM
- Selectable CAS latency (CL) for maximum compatibility
- Gold edge contacts
- Pb-free

## Module Specification

| Part Number          | Module Density & Configuration | Bandwidth | Data Rate | Timing (tCL-tRCD-tRP) |
|----------------------|--------------------------------|-----------|-----------|-----------------------|
| SP512MBLDU266O01(2)  | 512MB (64Mx64)<br>64Mx8 1Rank  | PC-2100   | DDR-266   | 2.5-3-3               |
| SP512MBLDU333O01(2)  |                                | PC-2700   | DDR-333   | 2.5-3-3               |
| SP512MBLDU400O01(2)  |                                | PC-3200   | DDR-400   | 3-3-3                 |
| SP001GBLDU266O01(2)  | 1GB (128Mx64)<br>128Mx8 2Ranks | PC-2100   | DDR-266   | 2.5-3-3               |
| SP001G BLDU333O01(2) |                                | PC-2700   | DDR-333   | 2.5-3-3               |
| SP001G BLDU400O01(2) |                                | PC-3200   | DDR-400   | 3-3-3                 |

Note:

1. This document supports all LDU Series DDR 184Pin UDIMM products.
2. Some item was being EOL in this list, Please contact with our sales Dep.
3. All part numbers end with a double-digit code is for customize use only.

Example: SP512MBLDU266O02-XX

## Pin Assignments

| 184-Pin DDR UDIMM Front |        |     |        |     |        |     |        |
|-------------------------|--------|-----|--------|-----|--------|-----|--------|
| Pin                     | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol |
| 1                       | VREF   | 24  | DQ17   | 47  | NC     | 70  | VDD    |
| 2                       | DQ0    | 25  | DQS2   | 48  | A0     | 71  | NC     |
| 3                       | VSS    | 26  | VSS    | 49  | NC     | 72  | DQ48   |
| 4                       | DQ1    | 27  | A9     | 50  | VSS    | 73  | DQ49   |
| 5                       | DQS0   | 28  | DQ18   | 51  | NC     | 74  | VSS    |
| 6                       | DQ2    | 29  | A7     | 52  | BA1    | 75  | CK2#   |
| 7                       | VDD    | 30  | VDDQ   | 53  | DQ32   | 76  | CK2    |
| 8                       | DQ3    | 31  | DQ19   | 54  | VDDQ   | 77  | VDDQ   |
| 9                       | NC     | 32  | A5     | 55  | DQ33   | 78  | DQS6   |
| 10                      | NC     | 33  | DQ24   | 56  | DQS4   | 79  | DQ50   |
| 11                      | VSS    | 34  | VSS    | 57  | DQ34   | 80  | DQ51   |
| 12                      | DQ8    | 35  | DQ25   | 58  | VSS    | 81  | VSS    |
| 13                      | DQ9    | 36  | DQS3   | 59  | BA0    | 82  | NC     |
| 14                      | DQS1   | 37  | A4     | 60  | DQ35   | 83  | DQ56   |
| 15                      | VDDQ   | 38  | VDD    | 61  | DQ40   | 84  | DQ57   |
| 16                      | CK1    | 39  | DQ26   | 62  | VDDQ   | 85  | VDD    |
| 17                      | CK1#   | 40  | DQ27   | 63  | WE#    | 86  | DQS7   |
| 18                      | VSS    | 41  | A2     | 64  | DQ41   | 87  | DQ58   |
| 19                      | DQ10   | 42  | VSS    | 65  | CAS#   | 88  | DQ59   |
| 20                      | DQ11   | 43  | A1     | 66  | VSS    | 89  | VSS    |
| 21                      | CKE0   | 44  | NC     | 67  | DQS5   | 90  | NC     |
| 22                      | VDDQ   | 45  | NC     | 68  | DQ42   | 91  | SDA    |
| 23                      | DQ16   | 46  | VDD    | 69  | DQ43   | 92  | SCL    |

| 184-Pin DDR UDIMM Back |        |     |        |     |        |     |        |
|------------------------|--------|-----|--------|-----|--------|-----|--------|
| Pin                    | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol |
| 93                     | VSS    | 116 | VSS    | 139 | VSS    | 162 | DQ47   |
| 94                     | DQ4    | 117 | DQ21   | 140 | NC     | 163 | NC     |
| 95                     | DQ5    | 118 | A11    | 141 | A10    | 164 | VDDQ   |
| 96                     | VDDQ   | 119 | DM2    | 142 | NC     | 165 | DQ52   |
| 97                     | DM0    | 120 | VDD    | 143 | VDDQ   | 166 | DQ53   |
| 98                     | DQ6    | 121 | DQ22   | 144 | NC     | 167 | NC     |
| 99                     | DQ7    | 122 | A8     | 145 | VSS    | 168 | VDD    |
| 100                    | VSS    | 123 | DQ23   | 146 | DQ36   | 169 | DM6    |
| 101                    | NC     | 124 | VSS    | 147 | DQ37   | 170 | DQ54   |
| 102                    | NC     | 125 | A6     | 148 | VDD    | 171 | DQ55   |
| 103                    | NC     | 126 | DQ28   | 149 | DM4    | 172 | VDDQ   |
| 104                    | VDDQ   | 127 | DQ29   | 150 | DQ38   | 173 | NC     |
| 105                    | DQ12   | 128 | VDDQ   | 151 | DQ39   | 174 | DQ60   |
| 106                    | DQ13   | 129 | DM3    | 152 | VSS    | 175 | DQ61   |
| 107                    | DM1    | 130 | A3     | 153 | DQ44   | 176 | VSS    |
| 108                    | VDD    | 131 | DQ30   | 154 | RAS#   | 177 | DM7    |
| 109                    | DQ14   | 132 | VSS    | 155 | DQ45   | 178 | DQ62   |
| 110                    | DQ15   | 133 | DQ31   | 156 | VDDQ   | 179 | DQ63   |
| 111                    | CKE1   | 134 | NC     | 157 | S0#    | 180 | VDDQ   |
| 112                    | VDDQ   | 135 | NC     | 158 | S1#    | 181 | SA0    |
| 113                    | NC     | 136 | VDDQ   | 159 | DM5    | 182 | SA1    |
| 114                    | DQ20   | 137 | CK0    | 160 | VSS    | 183 | SA2    |
| 115                    | A12    | 138 | CK0#   | 161 | DQ46   | 184 | VDDSPD |

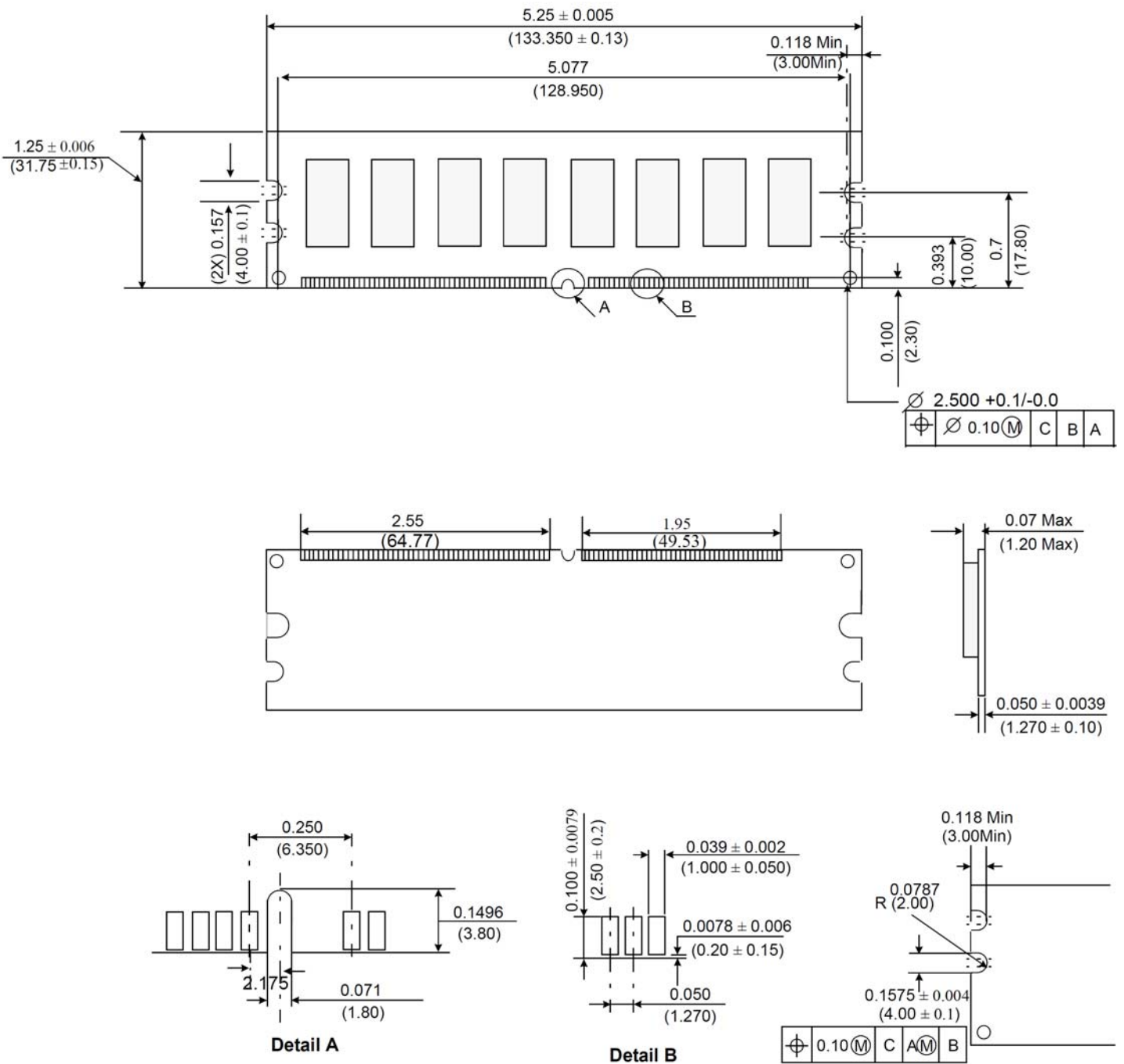
## Pin Description

| Symbol                                | Type   | Description   |
|---------------------------------------|--------|---|
| A0–A12                                | Input  | <b>Address inputs:</b> Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective device bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0, BA1) or all device banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command. |
| BA0–BA1                               | Input  | <b>Bank address:</b> BA0 and BA1 define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied.   |
| CK0, CK0#,<br>CK1, CK1#,<br>CK2, CK2# | Input  | <b>Clock:</b> CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data (DQ and DQS) is referenced to the crossings of CK and CK#.   |
| CKE0, CKE1                            | Input  | <b>Clock enable:</b> CKE (registered HIGH) activates and CKE (registered LOW) deactivates the internal clock, input buffers, and output drivers.  |
| RAS#, CAS#,<br>WE#                    | Input  | <b>Command inputs:</b> RAS#, CAS#, and WE# (along with S#) define the command being entered.  |
| S0#, S1#                              | Input  | <b>Chip select:</b> S# enables (registered LOW) and disables (registered HIGH) the command decoder.   |
| SA0–SA2                               | Input  | <b>Presence-detect address inputs:</b> These pins are used to configure the presence-detect devices.  |
| SCL                                   | Input  | <b>Serial clock for presence-detect:</b> SCL is used to synchronize the presence-detect data transfer to and from the module.   |
| SDA                                   | I/O    | <b>Serial presence-detect data:</b> SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.   |
| DM0–DM7                               | I/O    | <b>Input data mask:</b> DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins.   |
| DQ0–DQ63                              | I/O    | <b>Data input/output:</b> Bidirectional data bus.   |
| DQS0–DQS7,                            | I/O    | <b>Data strobe:</b> Output with read data, input with write data. DQS is edge aligned with read data, center-aligned with write data. Used to capture data.   |
| V <sub>DD</sub> /V <sub>DDQ</sub>     | Supply | <b>Power supply:</b> 2.5V ±0.1V.  |
| V <sub>DDSPD</sub>                    | Supply | <b>Serial EEPROM positive power supply:</b> +2.3V to +3.6V.   |
| V <sub>REF</sub>                      | Supply | SSTL_2 reference voltage. (V <sub>DD</sub> /2)  |
| V <sub>SS</sub>                       | Supply | Ground.   |
| NC                                    | –      | <b>No connect:</b> These pins are not connected on the module.  |

## Simplified Mechanical Drawing(x8 1Rank)

X64 DIMM, populated as one physical rank of x8 DDR SDRAMs

Units : Inches (Millimeters)



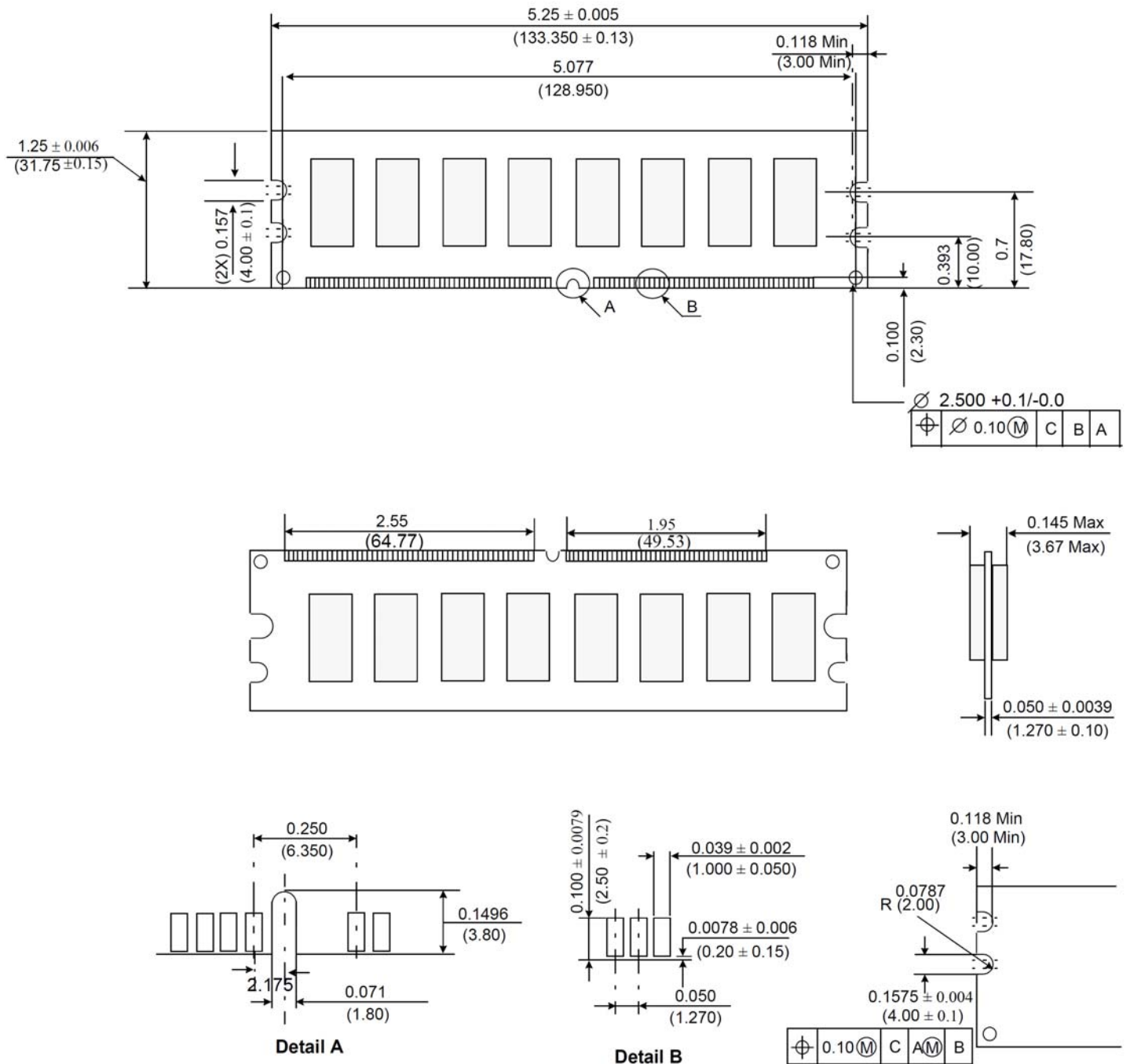
**Note:** 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

**Note:** 2. The dimensional diagram is for reference only.

## Simplified Mechanical Drawing(x8 2Ranks)

X64 DIMM, populated as two physical ranks of x8 DDR SDRAMs

Units : Inches (Millimeters)



**Note:** 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

**Note:** 2. The dimensional diagram is for reference only.